PERFORMANCE IMPROVEMENT IN POWERLINE CHANNEL USING TURBO CODE

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Abstract: **Power Line Communication (PLC) operates by impressing a modulated carrier over the wiring system conventionally used for delivering electricity. PLC eliminates the need for installing a dedicated cable for data transmission. Wide range of PLC techniques are available for different applications ranging from home automation to broadband communication.**

The use of turbo codes in Power Line Communication (PLC) system resulted in significant performance improvement. The present BER performance level of a turbo code scheme applied to a OFDM transmitter and PLC channel employing RSC (7,5) encoder, interleaver of size 4000 and code rate ½ ranges from 10^{-2} to 10^{-6} for the SNR ranging from 0 dB to 12 dB.

The performance of turbo code is better compared to other codes in power line channel as turbo code works efficiently with low SNR values. The Bit Error Rate reduced considerably with the use of turbo codes. Code rate, interleaver size and channel modulation scheme are the parameters that can be tuned in a turbo coding scheme to get better BER performance.

In this article I present a specification for a turbo code scheme applied to an OFDM transceiver on a PLC channel based on simulation results using a channel model impaired with AWGN and impulsive noise.

Keywords – Powerline communication; Turbo code; Biterror rate

I. INTRODUCTION

Power Line Communication (PLC) operates by impressing a modulated carrier over the wiring system conventionally used for delivering electricity. PLC eliminates the need for installing a dedicated cable for data transmission [1]. Wide range of PLC techniques is available for different applications ranging from home automation to broadband communication. Initially PLC technology was used only for voice communication (3 to 3.5 KHz). Today, PLC also finds applications in the field of broadband communication. Due to several limitations of PLC, frequency used is limited to 30 MHz. Since power lines were not designed for data communication, they act as a very harsh medium for high frequency signals. Major limitations of PLC include signal attenuation, noise and compatibility issues.

In PLC systems , wide variety of research is going on in many diverse areas such as PLC channel modelling, Broadband and Narrowband technologies, Noise effects, Communication Protocols, Low voltage indoor applications, suitable modulation technologies for different applications, Best coding scheme etc. Current research is more focused on forward error correction codes used in power line channel [8]. Many codes such as BCH codes, Low Density Parity Check Codes, Reed Solomon (RS) codes, Turbo codes etc are used in PLC. Among these performance of Turbo code is better for low SNR range which is ideal for PLC.

The BER performance can be improved by increasing the code rate, interleaver size and by using good channel modulation techniques. Channel response and noise in the in-home power-line channel are time varying, and show periodic patterns since electric devices, which are major noise sources, synchronously run with the ac-line cycle. Using the relatively stable channel characteristic of the power line, orthogonal frequency-division multiple access (OFDMA) schemes in power-line communications (PLCs) [3] can achieve multiuser diversity gain even in random access.

II. POWERLINE COMMUNICATION CHANNEL

The power-line channel has a frequency-selective characteristic [12]. Since there are many branches and taps in a power network, the transmitting signal is split so that the receiver receives multiple signals along with time differences, which makes the power-line channel frequency selective. In addition, since each power-line route between a pair of transmitters and receivers has different impedances and a various number of taps, each powerline channel has its own parameters, such as frequency-dependent response and rms delay spread.

The channel response periodically varies according to the AC line cycle. **Canete *et al***. in [4] have shown that the power line channel can be modeled as a linear periodically time-varying system since the impedance of electrical devices is time-variant. Because electrical devices in the power line generate cyclostationary noises that are synchronized with the AC line cycle, the channel response changes periodically. In time domain, **Umehara *et al***. in [9] have shown that the powerline channel periodically switches between two different channel responses.

There are two major noises in the power-line channel. One is the background noise from low-power noise sources, and the narrowband noise from wireless or wired sinusoidal signals. This type of noise shows a short-term time-varying behaviour, but it shows periodicity because noise sources are normally synchronous with the main ac frequency [4]. This noise is relatively stable and can be regarded as stationary for several minutes or even hours. The other one is the impulsive noise generated by electrical appliances, and it severely affects the communication signal.

III. INTRODUCTION TO TURBO CODES

A major advancement in coding theory occurred in 1993, when a group of researchers working in France developed turbo codes. The initial results showed that turbo codes could achieve energy efficiencies within only a half decibel of the Shannon capacity. This was an extraordinary result that at first was met with scepticism. But once other researchers began to validate the results independently, a massive research effort was soon underway with the goal of explaining and, better yet, enhancing the remarkable performance of turbo codes.

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A. Turbo Encoder

A turbo encoder consists of two convolutional encoders, connected in parallel, with an interleaver, and a "puncturing" stage. Convolutional encoders are often recursive systematic convolutional encoders (RSC) and look identical. The interleaver block permutes the input data in a pseudo-random order, to randomize the data stream, in such a way that the entry sequence to the second encoder is very different with respect to the original data stream. The block puncturing or perforating mechanism removes some parity bits to the output of each encoder with the aim of reducing the code rate and decrease the number of output symbols generated with respect to input data. As a result of this structure at the encoder, the output stream is composed of the original information data and parity bits generated by the two RSC encoders.

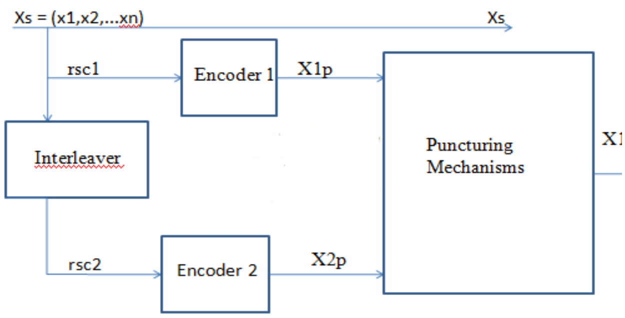

Fig.3.1 General Structure of Encoder[11].

B. Turbo Decoder

The general structure of a turbo decoder [11] is formed by a sequence of two MAP decoders, which are separated by one de-interleaving and one interleaver block, respectively. A feedback, from the second decoder to the first decoder produces a decoding gain as the iteration numbers increase. The figure shows the general structure of a turbo decoder using the BCJR-MAP algorithm.

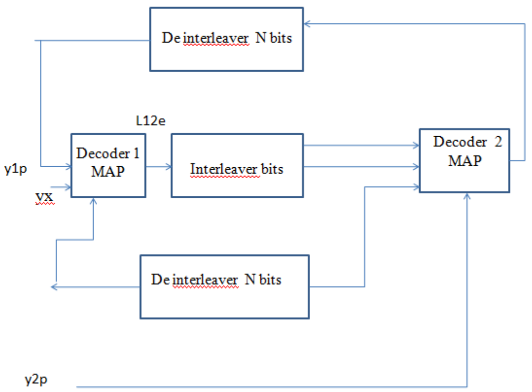

Fig 3.2: General structure of turbo decoder [11].

IV. TURBO CODES IN PLC CHANNEL

There have been several studies of channel turbo codes PLC implementation[10][11][6]. According to investigations, supplementing the OFDM modulation with this information coding technique has generated very good results in terms of bandwidth utilization making it more robust to errors caused by channel characteristics.

Some turbo code variants (i.e. different values for parameters) have been studied in order to compare their behaviour dealing with different conditions of noise and both time varying and frequency selective channels. Turbo code performance depends on noise variance fluctuation and the interleaver size.

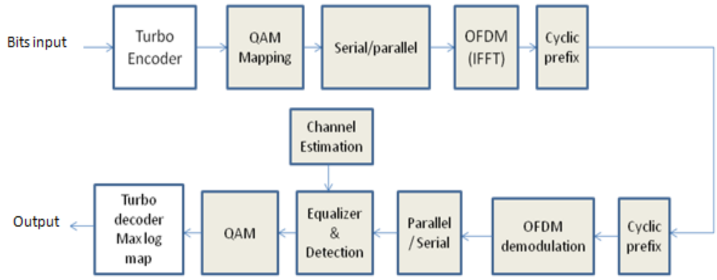

Fig 4.1. OFDM Transceiver in PLC

V. PROPOSED WORK - ERASURE TURBO CODE TECHNIQUE

A. RS Turbo Encoder Structure

The proposed turbo encoder, presented in Fig. 5.1, is composed of two identical RS (254,238) concatenated in a parallel structure, with a row/column block interleaver in between

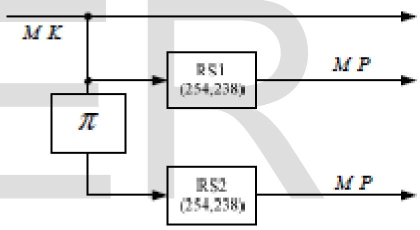

Fig.5.1 R S Turbo encoder structure

The interleaver size is *MK*, where *M* is its depth, and *K*=a number. The incoming data, of size *MK* symbols, is encoded by two identical RS encoders; each one generates *MP* parity check symbols. The code output has a size of *M(K+2P)* symbols, and the turbo code, as described below, is equivalent to a bloc code with a rate *K/K* + 2*P* since code components are identical.

B. Erasure Iterative Turbo Decoder

The decoder structure, similar to a classical turbo decoding one, consists of two RS decoders in cascade, as shown in Fig. 5.2

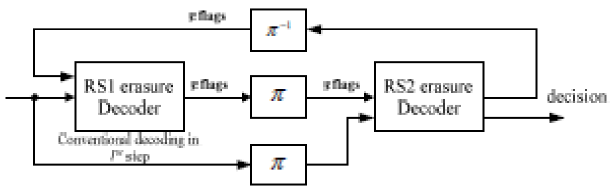

Fig.5.2 RS Turbo decoding structure

The two decoders corresponds to RS encoders in the turbo encoder, each of them carry out an erasure decoding, except the first

RS decoder which works in the conventional decoding manner during the first iteration. Error positions produced by the former decoder are used in the next erasure decoding.

The erasure decoding process is advantageous since it doubles the error correction capability. In fact, an RS (n, K) code can correct up to (n-K) erased symbols instead of $t =$ □ $n - K/2$ errors.

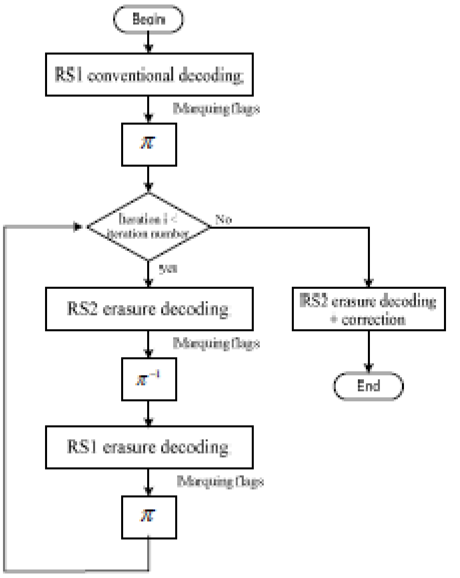

Fig.5.3 Iterative decoding flowchart of RS turbo code

In each decoding step, syndromes, the erasure locator polynomial and the error locator polynomial are computed to perform the erasure correction.

C. Erasure decoding algorithm

Variant alternatives are given in literature to decode using erasure information.
This procedure is summarized according the following steps [17]:

- Compute the erasure-locator polynomial using the erasure information provided by the receiver.
- Replace the erased coordinate with zeros and compute syndromes.
- Introduce a linear transformation on syndromes to compute "modified syndromes".
- Apply the Berlekamp algorithm using "modified syndromes" to find error-locator polynomial.
- Find roots of the error-locator polynomial and consequently the error locations decoding.
- Determine the magnitudes of errors and erasures using modified Forney algorithm.

V1 SIMULATION RESULTS

The BER Performance of the parallel concatenated RS codes have been evaluated by carrying out simulation of the complete PLC-OFDM system and is shown in fig 6.1 and 6.2..

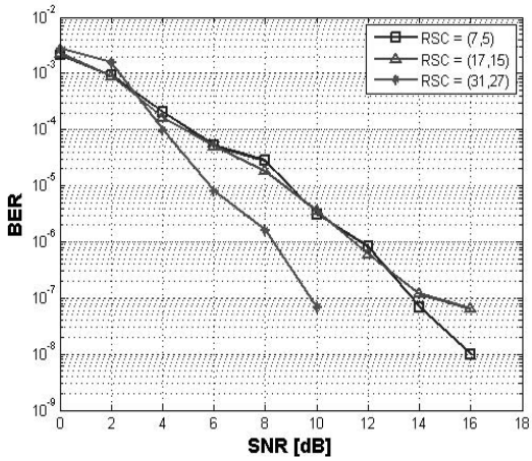

Fig 6.1 Performance for 3 variants of RSC encoders

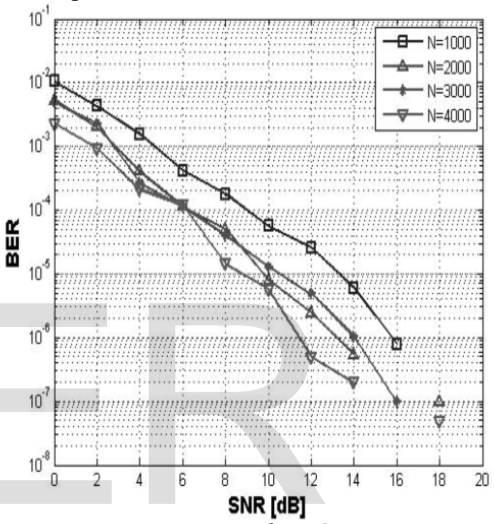

Fig:6.2. Comparison of interleaver sizes in PLC channel

V11. CONCLUSION

In this paper, we have investigated a new turbo coding schema using RS encoders with erasure decoding algorithm.

The decoding process is similar to conventional turbo decoding method, except that soft decision provided from one decoder to another is replaced by error flags information.

The proposed turbo code is used in order to correct burst errors generated by impulsive noise in PLC environment.

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